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A COMPARATIVE ANALYSIS OF DDR4 AND DDR5 MEMORY ARCHITECTURE

Endita Layla Sulistiyowati[1*], Aprillia Rahmasari Distiah[2], Nisa Ulin Ni'mah[3], Allifa Maulani[4], Aisyah Dwi Windarti[5], Noviara Zizi Amanda[6]
[1,2,3,4,5,6]Ahmad Dahlan University, Indonesia
[1] 2500018151@webmail.uad.ac.id

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ABSTRACT

The development of modern software demands high data transfer rates from the main memory. However, increasing conventional RAM speed is often hindered by thermal law limitations, triggering circuit temperature spikes due to forced clock speeds. This study aims to analyze DDR5 memory data bus path structural modifications in overcoming these semiconductor circuit physical limitations. The method employed is a literature study with a qualitative-descriptive approach, utilizing secondary data from Google Scholar, Garuda, and technical specification documents. The study scope is strictly confined to internal micro-architectural modifications, excluding memory capacity and density scaling parameters. Results indicate that increased data transfer rates in the DDR5 generation are achieved by restructuring the single 64-bit data bus path into a dual 32-bit sub-channel system. This modification combines with doubling the Burst Length value to BL16 to transmit large data packets simultaneously without frequent processor interruptions. In conclusion, this internal architectural engineering provides an effective solution to accelerate data transmission and maintain temperature stability without forcing memory physical frequency limits. Theoretically, these findings shift the memory optimization paradigm from frequency scaling to structural path efficiency, foundational for future scalable hardware designs.

Keywords: *Computer Architecture, DDR5 SDRAM, Dual Sub-channel, Burst Length, Thermal Management.*

INTRODUCTION

The increasingly complex development of modern software demands high computing performance from a computer system. Within the Von Neumann architecture, main memory or Random Access Memory (RAM) plays a crucial role as a bridge that synchronizes data communication between the processor and secondary storage media. However, the speed of data processing by the CPU has developed far more rapidly than the speed of RAM components in supplying that data. This massive performance gap between the two components triggers a data bottleneck phenomenon widely known in academia as the Von Neumann Bottleneck or memory bottleneck[1]. This issue has become one of the greatest challenges for computer architects to ensure that processor instructions are not stalled due to delays in the memory data supply, which ultimately drives a massive evolution in modern computer organization. As an initial mitigation step, the implementation of cache memory technology with high-level adaptive algorithms has been heavily adopted by the industry to reduce the impact of this memory wall and maintain the stability of data interaction [2].

In its development, the performance improvement of a RAM module is often

equated with an increase in the circuit clock frequency or clock speed, measured in Megahertz (MHz) [3]. However, continuously increasing the operating frequency of silicon circuits will inherently hit the physical limitations of modern semiconductor materials. Based on the laws of physics and thermodynamics, forcing extreme clock frequency increases has been proven to drastically trigger temperature spikes and heat dissipation in memory chips [4].

$$P = C \cdot V^2 \cdot f \quad (1)$$

P = total dynamic power dissipation
C = circuit load capacitance
V = voltage
f = component operating frequency (clock frequency)

Based on this equation, when the frequency (f) is forced to rise exponentially through overclocking methods, the power dissipation value (P) will increase linearly, which subsequently triggers a heat spike due to the Joule effect. Furthermore, forcing excessively high clock speeds also correlates negatively with energy efficiency because it causes massive electrical power consumption and risks degrading the stability of micro-data signal integrity within the circuit board [5]. Consequently, this absolute thermal ceiling of silicon substrates mandates that the semiconductor industry look beyond linear clock frequency scaling and pivot toward architectural path efficiency**.** Therefore, the conventional approach that relies solely on circuit frequency is considered no longer adequate to meet the computing needs of the next generation.

Based on these physical limitation characteristics, architects and semiconductor manufacturers have begun shifting their focus away from internal chip clock frequency as the sole indicator of performance. Current hardware design paradigms are geared more toward engineering internal path architectures to increase the overall data transfer rate, measured in MegaTransfers per second (MT/s) [6][7]. The implementation of Double Data Rate 5 (DDR5) memory technology, as specified by JEDEC, represents this architectural shift, where a single 64-bit channel is now split independently into two 32-bit sub-channels [7][8]. This modification allows the computer system to transfer a larger volume of data per second, even though the physical circuits within the semiconductor chip operate at a relatively stable base frequency. Through this approach, the total communication data flow capacity (bandwidth) can be continuously increased without straining the physical durability of the memory component itself.

Technically, the increase in data transfer speed within this modern memory architecture is achieved through two main internal logical structure modifications. The first change is made to the data bus path width of the computer's main memory module, where the single 64-bit wide channel used in the DDR4 generation is independently split into two sub-channel paths, each having a data width of 32 bits [7]. This new structure allows the processor to execute two different memory access commands simultaneously and independently on the same RAM module [1]. This architectural step serves to reduce the data instruction queue and minimize processor waiting time (latency). Through this architectural modification, the computer system can transmit a larger volume of data per second, thereby boosting overall performance speed. This mechanism forms the

theoretical foundation of why data transfer rate figures (MT/s) can increase beyond their physical circuit frequencies.

The writing of this article aims to analyze the structural modifications of the main memory data bus paths in overcoming the physical limitations of semiconductor circuit frequencies. The scope of the study in this article is limited to comparing the internal logical architectural characteristics between the DDR4 and DDR5 generations, specifically focusing on the aspects of transfer rate, sub-channel division, and the Burst Length mechanism. Ultimately, this theoretical study is expected to provide a structured academic understanding of the principles of engineering data communication paths in modern memory systems.

RESEARCH METHODS

The method used in writing this article is a literature study with a qualitative-descriptive approach. This research does not involve laboratory experiments or direct hardware testing, but rather focuses on collecting, analyzing, and synthesizing secondary data from various credible scientific sources.

Systematically, the workflow of this literature study is designed to address the memory performance gap presented in the introduction. The research procedure is divided into four main stages, which are illustrated in the Flowchart in Figure 1.

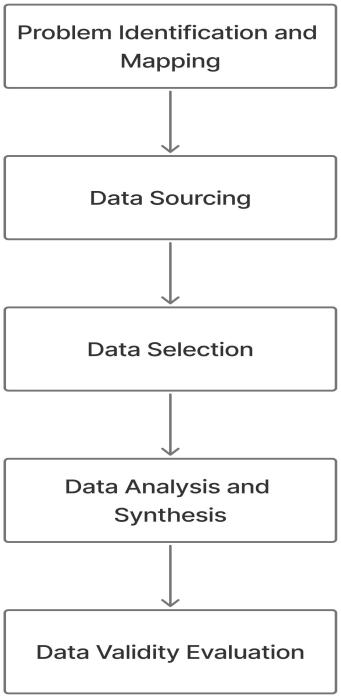

Figure 1 Research Process Flowchart

Problem Identification and Mapping

The initial stage begins with defining the scope of the theoretical study based on the Von Neumann Bottleneck phenomenon and thermal dissipation limits in semiconductor circuits. To maintain the focus of the discussion and

prevent it from expanding unnecessarily, the scope and parameters of this study are specifically limited as follows:

Research Scope (Limitations):

1. The study focuses on a comparative analysis of the internal logical architectural characteristics between DDR4 SDRAM and DDR5 SDRAM memory components.
2. The research is limited to circuit architectural solutions, thereby excluding discussions on memory capacity scale-up (Gigabytes) or the external physical aesthetics of the components (heatsinks).

Mapped Parameters:

1. Physical Frequency Characteristics (Clock Speed): Analyzing the threshold limits of modern semiconductor circuit frequencies in Megahertz (MHz) and their correlation with heat dissipation.
2. Data Communication Path Architecture: Mapping the structural efficiency of transitioning from a 64-bit single-channel data bus path (DDR4) to dual 32-bit sub-channels (DDR5).
3. Instruction Load Capacity (Burst Length): Evaluating the impact of doubling the data burst capacity from BL8 to BL16 on safely increasing the data transfer rate (MT/s).

Data Sourcing

The collection of literature data was conducted digitally through searches on the Google Scholar and Garba Rujukan Digital (Garuda) platforms, as well as technical specification documents from manufacturers. The criteria for data sources used in this paper are restricted based on the following provisions:

1. Publication Year Limit: Selected scientific articles and literature are prioritized to those published within the last 5 years (ranging from 2021 to 2026) to maintain the currentness of technical data regarding DDR5 memory developments.
2. Types of Data Sources:
    - Scientific journal articles or national and international seminar proceedings found through Google Scholar and Garuda, particularly in the topics of Informatics Engineering, Electrical Engineering, or Computer Architecture.
    - University textbooks regarding computer system organization and architecture.
    - Official standard specification documents published by semiconductor standardization organizations (JEDEC) and related hardware manufacturers as technical data references for DDR5 RAM.

Data Selection

This step was conducted to screen all the literature gathered from Google Scholar and Garuda to yield valid secondary data. The selection process was based on the following inclusion and exclusion criteria:

Inclusion Criteria (Accepted Articles):

1. The article must contain theoretical foundations or basic physical laws related to the impact of frequency increases on the temperature of digital

components.
2. The article must present quantitative data or structural visualizations regarding the comparison of DDR4 and DDR5 memory bus paths.
3. The literature must include a logical explanation of how micro-data processing mechanisms work, both in terms of channel partitioning and single-pass instruction load capacity.

Exclusion Criteria (Rejected Articles):

1. Articles discussing RAM technology in mobile devices (LPDDR) or graphics card memory (GDDR), as the focus of this assignment is solely on main computer memory (desktop/laptop).
2. Articles that do not include internal architectural analysis or only consist of brief reviews regarding hardware prices and market trends.

Data Analysis and Synthesis

The technical data collected from various literature articles were then categorized and analyzed based on the topic of discussion (thematic analysis). The data processing steps in writing this paper were performed as follows:

1. Comparative Data Synthesis: The author collected technical specification data from several literature sources and compiled them into a comparative table to clearly observe the parameter differences between DDR4 and DDR5 memory.
2. Cause-and-Effect Analysis: The author analyzed the rationale behind the circuit structural changes, specifically how modifications in data channel partitioning and Burst Length capacity can theoretically affect data transfer rate (MT/s) values.
3. Architectural Causality Analysis: The theoretical data was analyzed using a comparative-causal method to map out structural cause-and-effect relationships. Specifically, the analysis investigated how independent variables, such as memory channel partitioning (single 64-bit to dual 32-bit sub-channels) and Burst Length capacity expansion (BL8 to BL16), directly influence dependent performance outcomes, namely raw data transfer rates (MT/s), latency reduction, and thermal dissipation efficiency.
4. Descriptive Narrative Formulation: The results of the comparison and analysis were then synthesized into a coherent and structured written report to address the objectives of this Computer Architecture course assignment.

Data Validity Evaluation

The final stage of this research method is to evaluate all synthesized data and narratives. This evaluation process was carried out through the following two approaches:

- Cross-Checking and Validity Metrics: The author cross-examined data consistency by cross-matching experimental performance claims found in journal articles from Google Scholar and Garuda with the baseline technical data from official JEDEC specification documents. To evaluate data validity, specific quantitative metrics were utilized as reference baselines, including standard operating voltage thresholds (1.2V vs 1.1V),

maximum supported transfer rates (MT/s), burst configuration standards (BL16), and structural channel layouts. Any empirical data from literature that deviated from JEDEC's official hardware tolerance standards was discarded to ensure absolute data integrity.

- Assignment Alignment Review: The author re-evaluated the entire draft to ensure that the analysis presented remained strictly within the scope of computer circuit architecture and directly addressed the instructional goals of the Computer Architecture course.

RESULTS AND DISCUSSION

Comparative Technical Specifications of DDR4 and DDR5

The secondary data collection process conducted through the Google Scholar and Garuda platforms successfully gathered several technical documents and scientific articles relevant to memory hardware developments. From these literature sources, a number of key technical parameters were identified that differentiate the architectural characteristics between DDR4 and DDR5 memory generations. To facilitate the comparative analysis process in this literature study, the theoretical data and technical specifications obtained from various scientific documents are structurally summarized in Table 1 below.

Table 1 Architectural Comparison Between DDR4 and DDR5 SDRAM

Architectural Parameter	DDR4 SDRAM	DDR5 SDRAM
Base Circuit Frequency (Clock Speed)	1600 – 3200 MHz	2400 – 4400 MHz
Data Transfer Rate	1600 – 3200 MT/s	4800 – 8400 MT/s
Bus Path Architecture (Channel Layout)	1x 64-bit Channel	2x 32-bit Sub-channel
Data Burst Capacity (Burst Length)	BL8 / BC4	BL16 / BL8 / BC4
Operating Voltage	1.2 Volts	1.1 Volts

Based on the comparative data presented in Table 1, a significant leap in specifications from the DDR4 to the DDR5 generation is clearly visible. In terms of speed, DDR5 is capable of reaching transfer rates ranging from 4800 to 8400 MT/s, which far exceeds the maximum limit of DDR4 at 3200 MT/s. Aside from this raw speed increase, the most fundamental difference actually lies in the overhaul of its internal structure. DDR5 no longer utilizes a single 64-bit channel like DDR4, but instead splits it into two 32-bit sub-channels that operate independently. This change in path architecture is also balanced by doubling the data transmission capacity (Burst Length) from BL8 to BL16. Interestingly, despite offering much higher performance and data density, DDR5 successfully reduces its base

operating voltage requirement to 1.1 Volts from the previous 1.2 Volts in DDR4. This combination of parameter and structural changes serves as the primary key to overcoming performance bottlenecks in modern computing systems.

Analysis of Thermal Limits and Operating Voltage

An aggressive increase in clock speed within semiconductor components is proven to correlate directly with hardware temperature spikes. This aligns with the technical explanation provided by Intel in their educational article titled *"How to Overclock Your CPU from BIOS"*, which states that forcing a circuit to operate at a higher frequency directly and significantly raises the heat temperature of the silicon chip [9]. Therefore, the engineering behind lowering the standard voltage in DDR5 is a highly crucial step; looking at Corsair's technical explanation in the article *"RAM: Tips on safely overclocking memory"*, forcing a high voltage supply in pursuit of instant performance risks damaging internal circuitry and shortening the lifespan of the memory module itself [10].

This technological shift trend is further supported by the findings of a study titled "Manajemen Penyimpanan Sementara (RAM) Dan Pengelolaannya" (Temporary Storage Management (RAM) in Modern Electronic Devices). The journal notes that hardware developments from 2019 to 2023 show a significant adoption of DDR5 technology as a new strategy in temporary storage architecture [11]. This fact proves that upgrading to the latest generation of memory is indeed a primary necessity to keep pace with current computing demands. Consequently, engineering the standard operating voltage down to 1.1 Volts in the DDR5 era serves as a vital foundation.

In modern VLSI (Very Large Scale Integration) circuit design, mitigating high dynamic power dissipation is critical to preventing thermal throttling and maintaining micro-data signal integrity. Forcing higher clock speeds increases circuit noise and creates non-linear power-ground interference on the motherboard, which degrades electrical reliability [5]. Consequently, reducing the operating voltage to 1.1V in DDR5 serves as a fundamental physical baseline. According to memory architecture benchmarks, lowering the voltage significantly decreases the dynamic power scaling curve, allowing the silicon die to handle higher processing densities without triggering thermal stress or localized hot spots within the memory bank circuits [12]. This indicates that keeping component temperatures stable is paramount to avoiding system failures.

In light of these risks of physical damage from heat and voltage, the modern hardware industry has begun shifting its memory performance enhancement strategies. This characteristic is reinforced by Kingston in their technology review article titled *"Choosing Overclocked RAM: Aggressive Timings vs Higher Clock Speed"*, which explains that optimal data transfer speeds in next-generation memory do not necessarily have to be achieved by pushing the physical frequency limits of the circuit, but can instead be optimized through transmission density configurations (timings) and internal architectural efficiency. Accordingly, the regulation of lower base operating voltages implemented in the DDR5 era becomes an essential baseline that allows modern computer systems to operate substantially faster without compromising the stability of digital components [13].

Evolution of Memory Path Architecture from Single Channel to Dual Sub-channel

Through research titled "Studi Eksperimental Konsumsi RAM Selama Transfer Data Cloud Menggunakan Google Drive" (Experimental Study of RAM Consumption During Cloud Data Transfer Using Google Drive), it is established that intensive data transfer activities significantly drive up memory utilization to near-maximum capacity on entry-level devices, which ultimately causes a drastic drop in system responsiveness [14]. This degradation aligns with empirical benchmark data from software-level memory optimization studies, which confirm that inefficient execution paths and stagnant process allocations continuously stress the physical memory layer [15]. This condition of performance degradation and loss of responsiveness indirectly provides a strong indication of data queuing issues within conventional memory architectures.

In conventional memory architectures such as DDR4, communication with the CPU memory controller still relies on a single 64-bit wide channel. According to the findings in a study titled "Evolusi Arsitektur Komputasi dan Protokol Internet Awal: Analisis Historis Teknis Generasi Pertama" (Evolution of Computing Architecture and Early Internet Protocols: A Technical Historical Analysis of the First Generation), the foundational adoption of the Von Neumann Architecture in computer systems has, from the very beginning, focused heavily on pursuing universal data processing and transmission efficiency [16].

This issue is addressed more specifically by Hanif and Sugiantoro (2025) in their research titled "Literature Review: Evolusi Arsitektur Komputer dalam Konteks Sistem Organisasi Komputer" (Literature Review: The Evolution of Computer Architecture in the Context of Computer Organization Systems), which states that the physical limitations of the Von Neumann Architecture in the form of a memory bottleneck have been the primary driving factor behind the evolution of modern computer architecture, particularly regarding memory management and processor integration systems [1]. When the single 64-bit bus in conventional memory is forced to serve the data demands of highly rapid, modern multi-core processors, the path becomes congested and triggers latency that penalizes overall system performance. Therefore, these theoretical and empirical barriers underline the urgency for a radical overhaul toward a dual 32-bit sub-channel structure in the latest generation of memory.

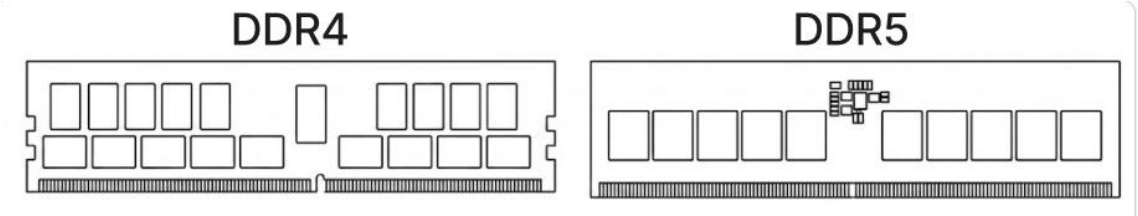

Figure 2 Comparison of DDR4 Single-Channel and DDR5 Dual Sub-channel Architecture

The tangible impact of this technological evolution is also reinforced by the results of a comparative study titled "ANALISIS PERFORMA PADA VIDEO GRAPHIC ARRAY (VGA) NVIDIA GTX 950M DDR3 DAN NVIDIA GTX 950M GDDR5" (Performance Analysis on Nvidia GTX 950M DDR3 and Nvidia GTX 950M GDDR5

Video Graphic Array (VGA)). The study reveals evidence that different generations of Double-Data-Rate (DDR) memory exert a massive influence on digital data processing speeds, even when circuits operate on the same data bus width [17]. This fact leads to the conclusion that computing systems can no longer rely solely on physical capacity, but are heavily dependent on the maturity of the component's logical architecture. If a generation upgrade in graphics memory alone can yield such a massive performance shift, then the decision to split the single 64-bit data bus in DDR4 into two independent 32-bit sub-channels in DDR5 stands as the most precise solution to eliminate the classic memory bottleneck inherited from the Von Neumann era.

Throughput Optimization Analysis Through Burst Length Expansion (BL16)

The implementation of DDR5 technology introduces a change to the Burst Length configuration, which is now increased to BL16, allowing the RAM to transmit data packets of 64 Bytes simultaneously without waiting for a new command from the processor. This principle of concurrent data burst transmission aligns with the experimental results in a study titled "Evaluasi Kinerja Mikrokontroler Low-Power dalam Penerapan Convolutional Neural Network untuk Kendali Lengan Prostetik Bionik" (Performance Evaluation of Low-Power Microcontrollers in Applying Convolutional Neural Networks for Bionic Prosthetic Arm Control). The journal notes that hardware-appropriate data processing based on the Amplitude of the First Burst (AFB) is proven to cut computation time down to just 41 milliseconds while saving power consumption [18]. This indicates that data burst models in hardware can indeed accelerate data transfers by reducing queue times within the circuitry. Therefore, the implementation of Burst Length 16 technology in DDR5 serves as an effective method to make RAM data transfers faster and more energy-efficient.

The operational mechanism of BL16 in this latest generation is also designed to reduce the frequency of new command interruptions from the processor while the RAM is transmitting 64-Byte data packets. This interruption issue concurs with simulation results in a study titled "Comparative Simulation: Four CPU Scheduling Algorithms with I/O Interruption Modeling Using OS-SIM". The journal reveals that the presence of interruptions within a computing system leads to longer data waiting times (Average Waiting Time) [19]. This demonstrates that excessively frequent interruptions in a computer system will inevitably degrade performance. Consequently, the application of Burst Length 16 technology in DDR5 becomes an effective way to minimize command interruptions, thereby allowing RAM data transfers to run faster and reducing data latency.

An increase in memory capacity is fundamentally performed to maintain system stability when processing heavy workloads. This is consistent with testing outcomes in a study titled "Analisis Pengaruh Peningkatan Kapasitas RAM Terhadap Performa Sistem Saat Menjalankan Aplikasi Berat" (Analysis of the Effect of Increasing RAM Capacity on System Performance When Running Heavy Applications). The journal states that larger RAM configurations consistently yield faster response times and more efficient power utilization in both rendering and gaming applications [20]. However, such performance gains reach a saturation point after touching a certain capacity threshold. This shows that optimizing

computer performance cannot solely rely on scaling up the capacity size in Gigabytes. Therefore, internal circuit architectural changes, such as those implemented in DDR5, stand as a more effective measure to break through these performance saturation limits without requiring continuous expansion of physical memory capacity.

CONCLUSION

Based on the results of the conducted literature study, it can be concluded that the transition from DDR4 to DDR5 memory architecture marks a fundamental paradigm shift in computer organization. The conventional approach of solely increasing silicon circuit frequencies has reached its absolute physical limits due to thermal laws, which inherently trigger severe temperature spikes, dynamic power dissipation, and degraded signal integrity. To address these boundaries, the substantial increase in data transfer rates (MT/s) in next-generation memory is successfully achieved through the structural engineering of internal circuit paths rather than relying on forced clock speeds. The implementation of a dual 32-bit sub-channel system combined with the doubling of Burst Length capacity to BL16 serves as the primary mechanism to multiply data communication bandwidth while safely maintaining hardware component temperature stability.

Looking forward, future memory architecture developments should extend beyond individual module optimization and focus on wider ecosystem scalability. Subsequent research and next-generation designs, such as the emerging DDR6 standards, should further refine sub-channel partitioning and power-management integration. Furthermore, exploring the integration of Compute Express Link (CXL) protocols is highly recommended to pioneer unified memory pooling and address modern data-intensive, multi-core computing demands without compromising hardware sustainability.

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